



1. GENERAL SPECIFICATION

1-1 Input Frequency Range	1340 MHz - 1450 MHz	
1-3 One Input Connector	F Fe-Male	
1-4 Nominal Input Impedance	75 Ohm	Note:
1-5 Tuning Circuit	Built-in PLL	SP5055
1-6 IF Frequency	479.50 MHz Center	(PLESSEY)
1-7 IF Bandwidth	27 MHz Nominal (Selectable)	Note:
1-8 Demodulation	Phase Locked Loop	TA8804F
1-9 Video Output Polarity	Positive Going	
1-10 Operating Voltage	+28V (+/-5%) +5V (+/-5%)	
1-11 Operating Temperature	-10°C ~ +60°C	
1-12 Operating Humidity	less than 80% R. H. (at 40°C)	
1-13 Storage Temperature	-20°C ~ +70°C	
1-14 Storage Humidity	less than 95% R. H. (at 40°C)	

2. STANDARD TEST CONDITION

test for electrical specification shall be preformed at following condition unless otherwise specified.

2-1 Ambient Condition	Temperature	25°C +/- 2°C
	Humidity	65% +/- 5% R. H.
	if no doubt on test results	
	Temperature	+5°C ~ +30°C
2-2 Measurement to Start	Humidity	45% ~ 80% R. H.
	could be applied	

2-2 Measurement to Start 30 minutes after DC power supplied

2-3 Power Supply

Terminal	Supply Voltage
+5V	+5V (+/-) 0.1V
+28V	+12V (+/-) 0.1V
SDA	specified tuning
SCL	pulse

3. CURRENT CONSUMPTION

Terminal	Min.	Typ.	Max.	Unit
+5V	190	240	290	mA
TU	0.5	1.0	3.0	mA

4. ABSOLUTE MAXIMUM VOLTAGE

Terminal	Max. Supply Voltage
LNB Power	DC +25V
+5V	DC +5.25V
TU	DC +30V
SDA,SCL	OV TO The Same Voltage AS +5V Terminal

Terminal	Max. Take Off Current
LNB Power	500mA
B. B. Output	0.5 mA

5. ELECTRICAL SPECIFICATION

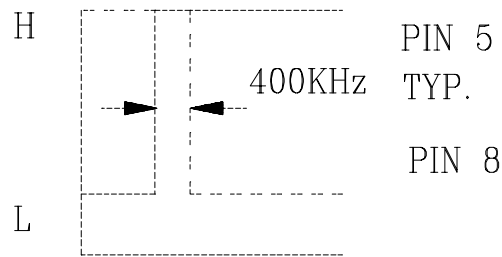
under standard test condition

Test Channel: DBS 20 CH

Input Level: -45 dBm

unless otherwise specified

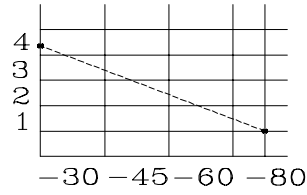
Condition	Min.	Typ.	Max.	Note
5-1 Input VSWR	1340 ~ 1450 MHz	2.0	3.0	
5-2 Noise Figure	1340 ~ 1450 MHz	8.0	12.	AGC fullgain dBm
5-3 Local Leakage at Input Terminal	1819.5~1929.5 MHz	-70.0	-63.0	dBm
5-4 Tuning Voltage Curve	1340 ~ 1450 MHz	5V	8V	
5-5 Local Oscillator +B Shift	tuning voltage shift with +B +/- 5%T		+/- 0.8	With tuing PLL locked
5-6 Local Oscillator Temperature Drift	Tuning voltage shift with -10°C ~ +60°C		+/- 1.3	V
5-7 IF 3dB Bandwidth	3dB down	27		MHz
5-8 AFT Output (2 bit Output)	Center Frequency Error (f0)	-2	+2	MHz



5-9 B. B. Output Characteristics

Condition	Min.	Typ.	Max.	Note
1) Video Output Level	video waveform white 100% PAL frequency deviation 16 MHz p-p without pre-emphasis			
white to SYNC	0.72	0.90	1.12	Vp-p
2) Gain-Frequency Response	test modulation frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 27 MHz			
Frequency Response		+/- 1	+/- 3	dB
3) Group Delay Response	test frequency: 60 Hz ~ 8 MHz without energy disposal modulation, reference frequency 100 KHz, IF BW: 27 MHz			
Group Delay		+/- 10	+/- 50	nsec
4) DG/DP	10 step siaircase 16MHz p-p PAL without energy disposal modulation, positive video amplifier with de-emphasis should be applied IF BW: 27 MHz			
DG (APL 50%)		4.0	8.0	%
DP (APL 50%)		3.0	5.0	deg
5) S/N	input C/N = 14 dB (Noise BW: 27 MHz) white 100% video 16 MHz p-p PAL with audio subcarrier modulation 3.4 MHz p-p DEV. @6.5 MHz positive video amplifier with de-emphasis should be applied 100 Hz ~ 5 MHz unweighted S/N, for power on reset indicator			
S/N	34.0	36.0		dB

7-1 Signal Level Out Voltage (V)
SIGNAL
LEVEL
OUT



INPUT LEVEL (dBM)

7-2 IIC Bus

1) SDA, SCL Input Voltage under standard test condition

Condition	Min.	Typ.	Max.	Note
High Voltage	3		5	V
Low Voltage	0		1.5	V

2) Address C2 (on write data format)

3) SDA, SCL Input Impedance SDA/SCL are in the high impedance and there should be no reliability problem with 5V continually on the SDA/SCL if power supply is switched off.

4) Date Format MSB LSB

	1	1	0	0	0	MA1	MA0	0	A	BYTE 1
Address	1	1	0	0	0	MA1	MA0	0	A	BYTE 1
Programmable Divider	0	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	A	BYTE 2
Programmable Divider	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	A	BYTE 3
Charge Pump and Test Bits	1	CP	T1	T0	1	1	1	OS	A	BYTE 4
I/O Port Control Bits	P7	P6	P5	P4	P3	P2	P1	P0	A	BYTE 5

table 1 write data format (MSB is transmitted first)

	1	1	0	0	0	MA1	MA0	1	A	BYTE1
Address	1	1	0	0	0	MA1	MA0	1	A	BYTE1
Status Byte	FOR	FL	I2	I1	I0	A2	A1	A0	A	BYTE 2

table 2 read data format

A: acknowledge bit

MA1, MA0: voltage address bits

CP: charge pump current select

T1: test mode selection

T0: charge pump disable

OS: varactor drive output disable switch

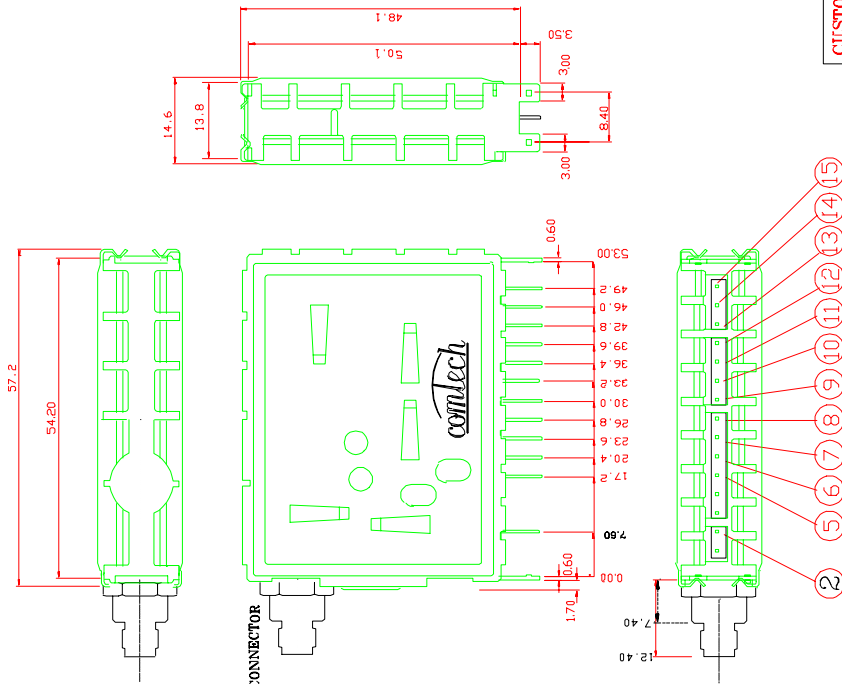
P7, P6, P5, P4, P3, P2, P1, P0: control output states

POR: power on reset indicator

I2, I1, I0: digital information from ports P7, P5 and P4

A2, A1, A0: 5 level ADC data from P6

PIN NO.	CONTENTS
1	—
2	LNB POWER
3	—
4	—
5	AFT OUT (DIGITAL)
6	+5V
7	B.B OUT
8	AFT OUT (DIGITAL)
9	SIGNAL LEVEL OUT
10	P4
11	12~28V
12	P3
13	P5
14	SDA
15	SCL



CUSTOM MODEL	FM1394RTIM
COMTECH MODEL	FM1394RTIM

NOTE 1.TOLERANCES ARE ± 0.5.
UNLESS OTHERWISE SPECIFIED.

DATE	SCALE	COMTECH TECHNOLOGY CO., LTD.
DESIGN	FILE	
CHKD.	APPD.	
DATE	UNIT	DOCUMENT No.
	mm	